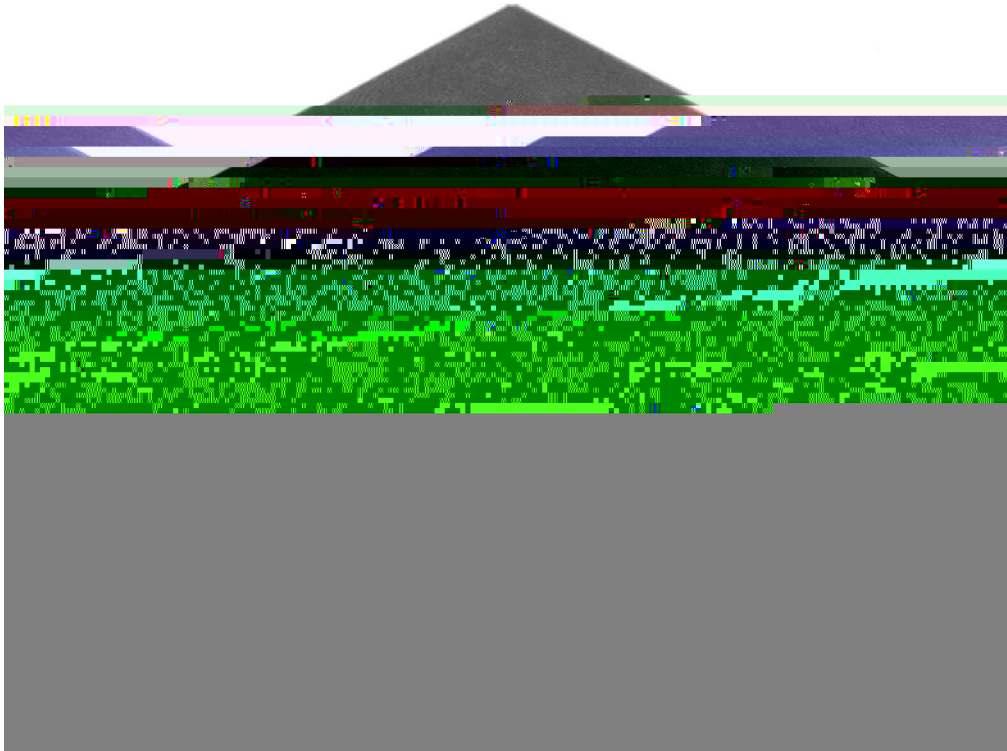




GPON ONU Triplexer Transceiver

RTXM170-601-C45

Features

- *Single Fiber Triplexer*
- *1.25Gbps data upstream / 2.5Gbps data downstream / 45~1002MHz CATV analog signal downstream*
- *Burst mode transmission with 1310nm DFB laser*
- *Continuous mode digital receiver with 1490nm APD-TIA*
- *Analog CATV receiver with 1555nm InGaAs PIN detector*
- *+3.3V / +12V power supply*
- *LVPECL compatible data input*
- *CML compatible data output*
- *CML transmitter burst-mode control*
- *LVTTTL I2C DDM interface*
- *LVTTTL TX_SD and RX_SD*
- *Soft Enable / Disable TX and Video*
- *Fully RoHS Compliant*
- *All metal housing for superior EMI performance*
- *Excellent ESD / TVS protection*
- *0℃ to 85℃ operating case temperature*
- *1×20 Pin and 2"×2" Package*
- *3PIN RF output connector*
- *Real time monitoring of:*
 - *Temperature*
 - *Supply voltage*
 - *Laser bias current*
 - *Transmitted optical power*
 - *Received optical power*
 - *Video Received optical power*
 - *RF Output level*

RTXM170-601-C45

Applications

- *GPON ONU Side*
- *Voice / Data / Video FTTx*

Standards

- *ITU-T G.984.2 Class B+*
- *ITU-T G.984.5*
- *SFF-8472 Rev 9.5*
- *RoHS 6*

Descriptions

°C

Block diagram

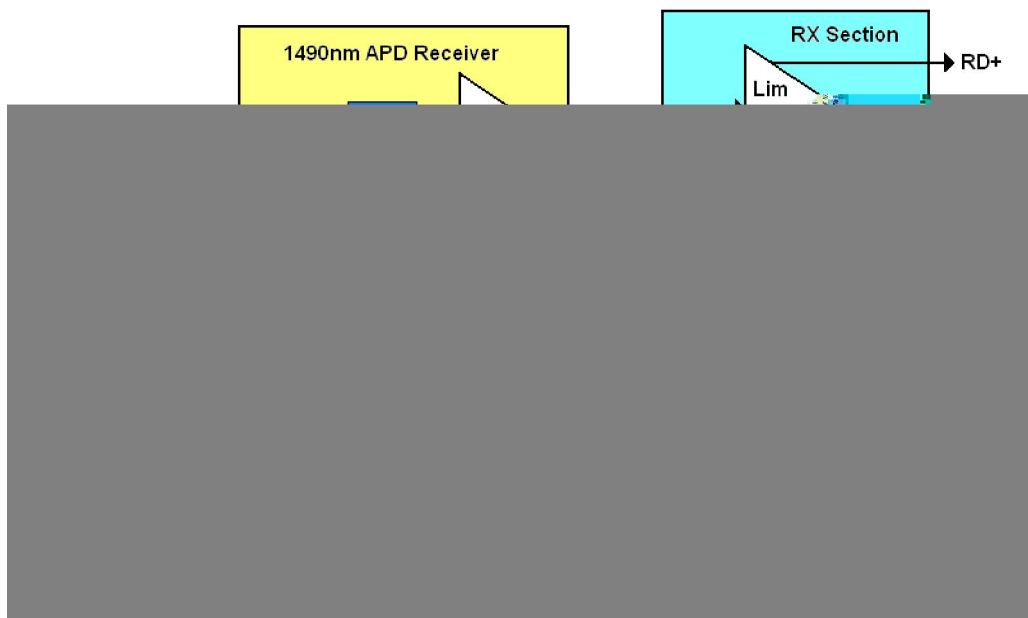


Figure 1

RTXM170-601-C45

Optical and Electrical Characteristics ($T_0 = 0^\circ\text{C}$ to $+85^\circ\text{C}$)

[illegible]

The diagram illustrates the internal architecture of the RTX170-601-C45 receiver. It is organized into two main functional blocks: the **Analog Receiver** and the **IIC Interface**.

Analog Receiver Section: This section is represented by a large light blue rectangle. It contains several internal components and signal paths:

- Input Stage:** The top of the block features a series of input lines, including a signal labeled **RF** and a **Reference** signal.
- Core Processing:** The central area of the block is filled with a complex network of lines and smaller, unlabeled blocks, representing the internal analog processing circuitry.
- Output Stage:** The bottom of the block shows output lines, including a signal labeled **IF** and a **Reference** signal.

IIC Interface Section: This section is represented by a smaller light blue rectangle located below the Analog Receiver block. It contains a single internal component and is connected to the main system bus.

System Bus: A horizontal line at the bottom of the diagram represents the system bus, which connects the IIC Interface to the rest of the system.

Note 2:

Note 4:

Note 6:

Note 8:

Note 10:

Note 13:

_____, (_____%)

Regulatory Compliance

Feature	Test Method	Performance

Ordering Information

Specifications		
Part No.		Application

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Note1 : ±

Note2 :