100Gb/s CFP2 Optical Transceiver

RTXM290-608

Features

- *Direct LC receptacle optical interface*
- *Single +3.3V power supply*
- *Hot-pluggable*
- *Operating optical data rate up to 112Gbps*
- *Transmission distance up to 40km*
- *AC coupling of CML signals*
- *1310 nm window cooled EA-DFB LD*
- *Integrated SOA、PIN ROSA and TOSA*
- *Low power dissipation(Max:9W)*
- *Built in digital diagnostic function*
- *Operating case temperature range:0℃ to 70℃*
- *Compliant with RoHs*
- *MDIO Communication Interface*

Application

- *Local and wide area network (LAN and WAN)*
- *Ethernet switches and router applications*
- *ITU-T OTU4 OTL4.4 applications*

Standards

Compliant with IEEE 802.3ba
Compliant with CFP2 MSA hardware specification,Version1.0 July 31,2014
Compliant with CFP MSA management specification，Version2.2July 01, 2013
Compliant with ITU-T G.959.1
Compliant with RoHS&WEEE

Absolute Maximum Ratings

Parameter	Symbol	Unit	Min	Max
Storage Temperature Range	Ts	°C	-40	+85
Relative Humidity	RH	%	5	85
Power Supply Voltage	Vcc	V	-0.5	+3.6
Operating Case Temperature Range	Tc	°C	-5	75
Receiver Damage Threshold Per Lane	P_{dag}	dBm	+5.5	

Recommended Operating Conditions

Parameter	Symbol	Unit	Min	Typ	Max
Operating Case Temperature Range	Tc	°C	0		70
	Vcc	V	3.2	3.3	3.4
		Gb/s		103.125	112

Output Low Voltage (I_{OL}=100uA)	3.3VOL	V			0.2	
Minimum Pulse Width of Control Pin Signal	t_CNTL	us	100			
1.2V LVCMOS Electrical Characteristics						
Input High Voltage	1.2VIH	V	0.84		1.5	
Input Low Voltage	1.2VIL	V	-0.3		0.36	
Input Leakage Current	1.2IIN	uA	-100		+100	
Output High Voltage	1.2VOH	V	1.0		1.5	
Output Low Voltage	1.2VOL	V	-0.3		0.2	
Output High Current	1.2IOH	mA			-4	
Output Low Current	1.2IOL	mA	+4			
Input Capacitance	Ci	pF			10	
Optical transmitter Characteristics						
Signaling Rate for Each Lane （100GbE）		Gbps	-	25.78125		
Signaling Rate for Each Lane （OTU4）				27.95249		
Four Lane Wavelength Range	λ1	nm	1294.53	1295.56	1296.59	
	λ2		1299.02	1300.05	1301.09	
	λ3		1303.54	1304.58	1305.63	
	λ4		1308.09	1309.14	1310.19	
Side Mode Suppression Ratio	SMSR	dB	30		-	
Total Average Launch Power	Pt	dBm	-		+8.9	
Average Launch Power for Each Lane	Pa	dBm	-2.5		+2.9	2
Optical Modulation Amplitude for Each Lane	OMA	dBm	-1.3		4.5	3
Transmitter and Dispersion Penalty for Each Lanes		TDP			1.5	
Average Launch Power of Off Transmitter for Each Lanes	Poff	dBm	-		-30	
Extinction Ratio	ER	dB	8			
$RIN_{20}OMA$		dB/Hz				

Management Interface Pins(MDIO)

The CFP Module supports alarm, control and monitor functions via an MDIO bus. The CFP MDIO pins are listed in the following table: Management Interface Pins

Management Interface Pins

Pin#	Symbol	Description	I/O	Logic	H	L	Pull-up/down
13	GLB_ALRMn	Global Alarm	I	3.3V LVCMOS	Ok	Alarm	
18	MDIO	Management Data Input Output Bi-Directional Data	I/0	1.2V LVCMOS			
17	MDC	MDIO Clock	I	1.2V LVCMOS			
19	PRTADR0	MDIO Physical Port address bit0	I	1.2V LVCMOS	per MDIO document[5]		
20	PRTADR1	MDIO Physical Port address bit1	I	1.2V LVCMOS			
21	PRTADR2	MDIO Physical Port address bit2	I	1.2V LVCMOS			

Hardware Signaling Pin Timing Requirements

Timing Parameters for CFP hardware Signal Pins are listed in the following table.

Timing Parameters for CFP hardware Signal Pins

Parameter	Symbol	Min	Max	Units	Notes&Conditions
Hardware MOD_LOPWR assert	t_MOD_LOPWR_assert		1	ms	Application Specific May depend on current state Condition when signal is applied .See

Time					"OR" of Associated MDIO alarm& status registers.Please see MDIO document for further details
Global Alarm De-assert Delay Time	GLB_ALRMn_deassert		150	ms	This is a logical "OR" of Associated MDIO alarm& status registers.Please see MDIO document for further details
Management Interface Clock Period	t_prd	250		ns	MDC is 4MHz rate
Host MDIO t_setup	t_setup	10		ns	
Host MDIO t_hold	t_hold	10		ns	
CFP MDIO t_delay	t_delay	0	175	ns	
Initialization time from Reset	t_initialize		2.5	s	
Transmitter Disabled(TX_DIS_asserted)	t_deassert		100	us	Application Specific
Transmitter Enabled(TX_DIS_asserted)	t_assert		20	ms	Value is dependent upon module start-up time.Please See register "Maximum TX-Turn-on Time" in "CFP MSA Management Interface Specification"

High Speed Electrical Characteristics

Reference Clock Characteristics（optional）

		Min	Typ	Max	Unit	Notes
Impedance	Zd	80	100	120	Ω	
Frequency			161.1328125/644.53125		MHz	1/160 or 1/40 of electrical lane rate（100GE）
			174.7031 /698.8123MHz			1/160 or 1/40 of electrical lane rate（OTU4）
Frequency Stability	△f	-100		100	ppm	For Ethernet applications
		-20		20		For Telecom applications
Output	V_{DIFF}	400		1200	mV	Peak to Peak

Differential Voltage						Differential
RMS jitter[1,2]	σ			10	ps	Random Jitter Over frequency band of 10KHz<f<10MHz
Clock Duty Cycle		40		60	%	
Clock Rise/Fall Time 10%/90%	$t_{r/f}$	200		1250	ps	1/64 of electrical lane rate
		50		315		1/16 of electrical lane rate

Optional Transmitter and Receiver Monitor Clock Characteristics

		Min	Typ	Max	Unit	Notes
Impedance	Zd	80	100	120	Ω	
Frequency					MHz	1/8 of Network lane rate
Output Differential Voltage	V_{DIFF}	400		1200	mV	Peak to Peak Differential
Clock Duty Cycle		40		60	%	

CFP Register Allocation

CFP Register Allocation					
Staring Address in Hex	Ending Address in Hex	Access Type	Allocated Size	Data Bit Width	Table Name and Description
0000	7FFF	N/A	32768	N/A	Reserved for IEEE 802.3 use
8000	807F	RO	128	8	CFP NVR 1.Basic ID register
8080	80FF	RO	128	8	CFP NVR 2.Extended ID register
8100	817F	RO	128	8	CFP NVR 3. Network lane specific registers
8180	81FF	RO	128	8	CFP NVR 4
8200	83FF	RO	4x128	N/A	MSA Reserved
8400	847F	RO	128	8	Vendor NVR 1. Vendor data registers
8480	84FF	RO	128	8	Vendor NVR 2. Vendor data registers
8500	87FF	RO	6x128	N/A	Reserved by CFP MSA
8800	887F	R/W	128	8	User NVR 1. User data registers
8880	88FF	R/W	128	8	User NVR 2. User data registers
8900	8EFF	RO	12x128	N/A	Reserved by CFP MSA
8F00	8FFF	N/A	2x128	N/A	Reserved for User private use
9000	9FFF	RO	4096	N/A	Reserved for vendor private use
A000	A07F	R/W	128	16	CFP Module VR1. CFP Module level control and DDM registers
A080	A0FF	RO	128	16	Reserved by CFP MSA
A100	A1FF	RO	2x128	N/A	Reserved by CFP MSA
A200	A27F	R/W	128	16	etwork Lane VR 1.Network lane specific

B000	FFFF	RO	5x4096	N/A	Reserved by CFP MSA

CFP NVR1

CFP NVR1

Hex Addr	Size	Access Type	Bit	Register Name	Content (HEX)	LSB Unit
Base ID Information						
8000	1	RO	7~0	Module Identifier	11	N/A
8001				Extended Identifier	A4	N/A
8002	1	RO	7~0	Connector Type Code	7	N/A
8003	1	RO	7~0	Ethernet Application Code	2	N/A
8004	1	RO	7~0	Fiber Channel Application Code	0	N/A
8005	1	RO	7~0	Copper Link Application Code	0	N/A
8006	1	RO	7~0	SONET/SDH Application Code	0	N/A

806E	1	RO	7~0	Digital Diagnostic Monitoring Type	C	N/A
806F	1	RO	7~0	Digital Diagnostic Monitoring Capability 1	3	N/A
8070	1	RO	7~0	Digital Diagnostic Monitoring Capability 2	F	

80BA	2	RO	7~0	Laser Temperature High Warning Threshold	3C	SeeA2C0h
80BC	2	RO	7~0	Laser Temperature Low Warning Threshold	28	SeeA2C0h
80BE	2	RO	7~0	Laser Temperature Low Alarm Threshold	23	SeeA2C0h
80C0	2	RO	7~0	Receive Optical Power High Alarm Threshold	AE7C	SeeA2D0h
80C2	2	RO	7~0	Receive Optical Power High Warning Threshold	6E18	SeeA2D0h
80C4	2	RO	7~0	Receive Optical Power Low Warning Threshold	51	SeeA2D0h
80C6	2	RO	7~0	Receive Optical Power Low Alarm Threshold	33	SeeA2D0h
80C8	55	RO	7~0	Reserved	0	TBD
80FF	1	RO	7~0	CFP NVR 2 Checksum	2E	N/A

CFP NVR3

Network Lane BOL Measurement Registers

Hex Addr	Size	Access Type	Bit	Register Name	Content (HEX)	LSB Unit
Base ID Information						
8100	32	RO	7~0	Rx Sensitivity Spec for network lanes 0~15	F9	0.01dBm
8120	32	RO	7~0	Tx Power Spec for network lanes 0~15	FF	0.01dBm
8140	32	RO	7~0	Measured ER for network lanes 0~15	3	0.01dB
8160	32	RO	7~0	Path Penalty for network lanes 0~15	0	0.01dB

CFP NVR4

Hex Addr	Size	Access Type	Bit	Register Name	Content (HEX)	LSB Unit
Base ID Information						
8180	1	RO	7~0	CFP NVR3 Checksum	E	N/A
8181	127	RO	7~1	Reserved	0	10m

CFP VR1

Hex Addr	Size	Access Type	Bit	Register Name	Content (HEX)	LSB Unit
Module Command/Setup Registers						
A000	2	RO	15~0			

		RW	7~0	Alarm Source Code		
A009	1	RO		**PRG_ALRM2 Source Select**	0002h	
			15~8	Reserved		
		RW	7~0	Alarm Source Code		
A00A	1	RO		**PRG_ALRM1 Source Select**	0001h	
			15~8	Reserved	00h	
		RW	7~0	Alarm Source Code	00h	
A00B	1	RO		Module Bi-/Uni-Directional Operating Mode Select	0000h	
			15~3	Reserved	0	
		RW	2~0	Module Bi/uni-Direction Mode Select	00b	
A00C	4	RO		Reserved	0000h	
Module Control Registers						
A010	1			**Module General Control**	0000h	
		RW/SC/LH	15	Soft Module Reset	0	
		RW	14	Soft Module Low Power	0	
		RW	13	Soft TX Disable	0	
		RW	12	Soft PRG_CNTL3 Control	0	
		RW	11	Soft PRG_CNTL2 Control	0	
		RW	10	Soft PRG_CNTL1 Control	0	
			9	Soft GLB_ALRM Test		

A013	1	RW		**Individual Network Lane TX_DIS Control**	0000h	
			15	Lane 15 Disable	0	
			14	Lane 14 Disable	0	
			13	Lane 13 Disable	0	
			12	Lane 12 Disable	0	
			11	Lane 11 Disable	0	
			10	Lane 10 Disable	0	
			9	Lane 9 Disable	0	
			8	Lane 8 Disable	0	
			7	Lane 7 Disable	0	
			6	Lane 6 Disable	0	
			5	Lane 5 Disable	0	
			4	Lane 4 Disable	0	
			3	Lane 3 Disable	0	
			2	Lane 2 Disable	0	
			1	Lane 1 Disable	0	
			0	Lane 0 Disable	0	

A014

				Summary		
			9	Module Fault Summary	0	
			8	Module General Status Summary	0	
			7	Module State Summary	0	
			6~1	Reserved	0	
			0	Soft GLB_ALRM Test Status	0	
A019	1	RO		**Network Lane Alarm and Warning Summary**	0000h	
			15	Lane 15 Alarm and Warning Summary	0	
			14	Lane 14 Alarm and Warning Summary	0	
			13	Lane 13 Alarm and Warning Summary	0	
			12	Lane 12 Alarm and Warning Summary	0	
			11	Lane 11 Alarm and Warning Summary	0	
			10	Lane 10 Alarm and Warning Summary	0	
			9	Lane 9 Alarm and Warning Summary	0	
			8	Lane 8 Alarm and Warning Summary	0	
			7	Lane 7 Alarm and Warning Summary	0	
			6	Lane 6 Alarm and Warning Summary	0	
			5	Lane 5 Alarm and Warning Summary	0	
			4	Lane 4 Alarm and Warning Summary	0	
			3	Lane 3 Alarm and Warning Summary	0	
			2	Lane 2 Alarm and Warning Summary	0	
			1	Lane 1 Alarm and Warning Summary	0	
			0	Lane 0 Alarm and Warning Summary	0	
A01A	1	RO		**Network Lane Fault and Status Summary**	0000h	
			15	Lane 15 Fault and Status Summary	0	
			14	Lane 14 Fault and Status Summary		

			8	Lane 8 Fault and Status Summary	0	
			7	Lane 7 Fault and Status Summary	0	
			6	Lane 6 Fault and Status Summary	0	
			5	Lane 5 Fault and Status Summary	0	
			4	Lane 4 Fault and Status Summary	0	
			3	Lane 3 Fault and Status Summary	0	
			2	Lane 2 Fault and Status Summary	0	
			1	Lane 1 Fault and Status Summary	0	
			0	Lane 0 Fault and Status Summary	0	
A01C	1	RO		Reserved	0	
Module FAWS Registers						
A01D	1	RO		**Module General Status**	0000h	
			15	Reserved	0	
			14	Reserved	0	
			13	HW_Interlock	0	
			12~11	Reserved	0	
			10	Loss of REFCLK Input	0	
			9	TX_JITTER_PLL_LOL	0	
			8	TX_CMU_LOL	0	
			7	TX_LOSF	0	
			6	TX_HOST_LOL	0	
			5	RX_LOS	0	
			4	RX_NETWORK_LOL	0	
			3	Out of Alignment	0	
			2	Reserved	0	
			1	HIPWR_ON	0	
			0	Reserved	0	
A01E	1	RO		**Module Fault Status**	0000h	
			15	Reserved	0	
			14~7	Reserved	0	
			6	PLD or Flash Initialization Fault	0	
			5	Power Supply Fault	0	
			4~2	Reserved	000b	
			1	CFP Checksum Fault	0	
			0	Reserved	0	
A01F	1	RO		**Module Alarms and Warnings 1**	0000h	
			15~12	Reserved	000b	
			11	Mod Temp High Alarm	0	
			10	Mod Temp High Warning	0	
			9	Mod Temp Low Warning	0	
			8	Mod Temp Low Alarm	0	
			7	Mod Vcc High Alarm	0	
			6	Mod Vcc High Warning	0	
			5	Mod Vcc Low Warning	0	
			4	Mod Vcc Low Alarm	0	
			3	Mod SOA Bias High Alarm	0	
			2	Mod SOA Bias High Warning	0	
			1	Mod SOA Bias Low Warning		

			2	Mod Aux 2 High Warning	0	
			1	Mod Aux 2 Low Warning	0	
			0	Mod Aux 2 Low Alarm	0	
A021	1	RO		Reserved	0000h	
A022	1			**Module State Latch**	0000h	
		RO	15~9	Reserved	0	
		RO/LH/COR	8	High-Power-down State Latch	0	
		RO/LH/COR	7	TX-Turn-off State Latch	0	
		RO/LH/COR	6	Fault State Latch	0	
		RO/LH/COR	5	Ready State Latch	0	
		RO/LH/COR	4	TX-Turn-on State Latch	0	
		RO/LH/COR	3	TX-Off State Latch	0	
		RO/LH/COR	2	High-Power-up State Latch	0	
		RO/LH/COR	1	Low-Power State Latch	0	
		RO/LH/COR	0	Initialize State Latch	0	
A023	1			**Module General Status Latch**	0000h	
		RO	15	Reserved	0	
		RO	14	Reserved	0	
		RO/LH/COR	13	HW_Interlock Latch	0	
		RO	12~11	Reserved	0	
		RO/LH/COR	10	Loss of REFCLK Input Latch	0	
		RO/LH/COR	9	TX_JITTER_PLL_LOL Latch	0	
		RO/LH/COR	8	TX_CMU_LOL Latch	0	
		RO/LH/COR	7	TX_LOSF Latch	0	
		RO/LH/COR	6	TX_HOST_LOL Latch	0	
		RO/LH/COR	5	RX_LOS Latch	0	
		RO/LH/COR	4	RX_NETWORK_LOL Latch	0	
		RO/LH/COR	3	Out of Alignment Latch	0	
		RO	2~0	Reserved	000b	
A024	1			**Module Fault Status latch**	0000h	
		RO	15~7	Reserved	0	
		RO/LH/COR	6	PLD or Flash Initialization Fault Latch	0	
		RO/LH/COR	5	Power Supply Fault Latch	0	
		RO	4~2	Reserved	000b	
		RO/LH/COR	1	CFP Checksum Fault Latch	0	
		RO	0	Reserved	0	
A025	1			**Module Alarms and Warnings 1 Latch**	0000h	
		RO	15~12	Reserved	0000b	
		RO/LH/COR	11	Mod Temp High Alarm Latch	0	
		RO/LH/COR	10	Mod Temp High Warning Latch	0	
		RO/LH/COR	9	Mod Temp Low Warning Latch	0	
		RO/LH/COR	8	Mod Temp Low Alarm Latch	0	
		RO/LH/COR	7	Mod Vcc High Alarm Latch	0	
		RO/LH/COR	6	Mod Vcc High Warning Latch	0	
		RO/LH/COR	5	Mod Vcc Low Warning Latch	0	
		RO/LH/COR	4	Mod Vcc Low Alarm Latch	0	
		RO/LH/COR	3	Mod SOA Bias High Alarm Latch	0	
		RO/LH/COR	2	Mod SOA Bias High Warning Latch	0	
		RO/LH/COR	1	Mod SOA Bias Low Warning Latch	0	
		RO/LH/COR	0	Mod SOA Bias Low Alarm Latch	0	
A026	1			**Module Alarms and Warnings 2 latch**	0	
		RO	15~8	Reserved	0	
		RO/LH/COR	7	Mod Aux 1 High Alarm Latch	0	
		RO/LH/COR	6	Mod Aux 1 High Warning Latch	0	

		RO/LH/COR	5	Mod Aux 1 Low Warning Latch	0	
		RO/LH/COR	4	Mod Aux 1 Low Alarm Latch	0	
		RO/LH/COR	3	Mod Aux 2 High Alarm Latch	0	
		RO/LH/COR	2	Mod Aux 2 High Warning Latch	0	
		RO/LH/COR	1	Mod Aux 2 Low Warning Latch	0	
		RO/LH/COR	0	Mod Aux 2 Low Alarm Latch	0	
A027	1	RO		Reserved	0000h	
A028	1			**Module Stable Enable**	006Ah	
		RO	15~9	Reserved	0	
		RW	8	High-Power-down State Enable	0	
		RW	7	TX-Turn-off State Enable	0	

A02C	1			**Module Alarms and Warnings Enable**	**00FFh**	
		RO	15~8	Reserved	00h	
		RW	7	Mod Aux 1 High Alarm Enable	1	
			6	Mod Aux 1 High Warning Enable	1	
			5	Mod Aux 1 Low Warning Enable	1	
			4	Mod Aux 1 Low Alarm Enable	1	
			3	Mod Aux 2 High Alarm Enable	1	
			2	Mod Aux 2 High Warning Enable	1	
			1	Mod Aux 2 Low Warning Enable	1	
			0	Mod Aux 2 Low Alarm Enable	1	
A02D	2	RO		Reserved	0000h	
Module Analog A/D Value Registers						
A02F	1	RO	15~0	Module Temp Monitor A/D Value	0000h	
A030	1	RO	15~0	Module Power supply	0000h	
				3.3 V Monitor A/D Value	0000h	
A031	1	RO	15~0			

A210	16	RO		**Network Lane n Fault and Status**	0000h	
			15	Lane TEC Fault	0	
			14	Lane Wavelength Unlocked Fault	0	
			13	Lane APD Power Supply Fault	0	
			12~8	Reserved	0	
			7	Lane TX_LOSF	0	
			6	Lane TX_LOL	0	
			5	Reserved	0	
			4	Lane RX_LOS	0	
			3	Lane RX_LOL	0	
			2	Lane RX FIFO error	0	
			1	Reserved	0	
			0	Reserved	0	
Network Lane FAWS Latch Registers						
A220	16	RO/LH/COR		**Network Lane n Alarm and Warning Latch**	0000h	
			15	Bias High Alarm Latch	0000h	
			14	Bias High Warning Latch	0	
			13	Bias Low Warning Latch	0	

CFP Host lane Lane VR1

Host Lane VR1

Host Lane VR1						
Hex Addr	Size	Access Type	Bit	Register Name	Content (HEX)	LSB Unit
Host Lane FAWS Status Registers						
A400	16			**Host Lane m Fault and Status**	0000h	
		RO	15~2	Reserved	0	
		RO	1	Lane TX FIFO Error	0	
		RO	0	TX_HOST_LOL	0	
Host Lane FAWS Latch Registers						
A410	16			**Host Lane m Fault and Status Latch**	0000h	
		RO	15~2	Reserved	0	
		RO/LH/COR	1	Lane TX FIFO Error Latch	0	
		RO/LH/COR	0	TX_HOST_LOL Latch	0	

Table : CFP2 Pin-Map

1	GND
2	*(TX_MCLKn)*
3	*(TX_MCLKp)*
4	GND
5	N.C.
6	N.C.
7	3.3V_GND
8	3.3V_GND
9	3.3V
10	3.3V
11	3.3V
12	3.3V
13	3.3V_GND
14	3.3V_GND
15	VND_IO_A
16	VND_IO_B
17	PRG_CNTL1
18	PRG_CNTL2
19	PRG_CNTL3
20	PRG_ALRM1
21	PRG_ALRM2
22	PRG_ALRM3
23	GND

104	GND
103	N.C.
102	N.C.
101	GND
100	TX3n
99	TX3p
98	GND
97	TX2n
96	TX2p
95	GND
94	N.C.
93	N.C.
92	GND
91	N.C.
90	N.C.
89	GND
88	TX1n
87	TX1p
86	GND
85	TX0n
84	TX0p
83	GND
82	N.C.

24	TX_DIS	81	N.C.
25	RX_LOS	80	GND
26	MOD_LOPWR	79	*(REFCLKn)*
27	MOD_ABS	78	*(REFCLKp)*
28	MOD_RSTn	77	GND
29	GLB_ALRMn	76	N.C.
30	GND	75	N.C.
31	MDC	74	GND
32	MDIO	73	RX3n
33	PRTADR0	72	RX3p
34	PRTADR1	71	GND
35	PRTADR2	70	RX2n
36	VND_IO_C	69	RX2p
37	VND_IO_D	68	GND
38	VND_IO_E	67	N.C.
39	3.3V_GND	66	N.C.
40	3.3V_GND	65	GND
41	3.3V	64	N.C.
42	3.3V	63	N.C.
43	3.3V	62	GND
44	3.3V	61	RX1n
45	3.3V_GND	60	RX1p
46	3.3V_GND	59	GND
47	N.C.	58	RX0n
48	N.C.	57	RX0p
49	GND	56	GND
50	*(RX_MCLKn)*	55	N.C.
51	*(RX_MCLKp)*	54	N.C.
52	GND	53	GND

Table: Pin description

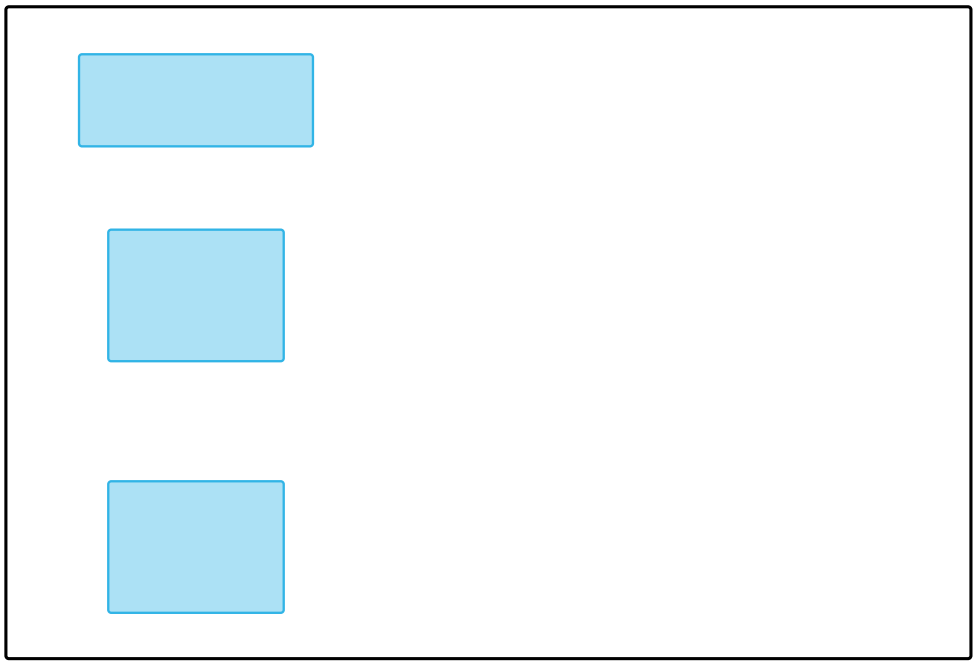
PIN#

	N.C.			No Connect
6	N.C.			No Connect
7	3.3V_GND			3.3V Module Supply Voltage Return Ground,can be separate or tied together with Signal
8	3.3V_GND			
9	3.3V			3.3V Module Supply Votage
10	3.3V			

35	**PRTADR2**	I	1.2V CMOS	MDIO Physical Port address bit 2
36	**VND_IO_C**	I/O		Module Vendor I/O C. Do Not Connect!
37	**VND_IO_D**	I/O		Module Vendor I/O D. Do Not Connect!
38	**VND_IO_E**	I/O		Module Vendor I/O E. Do Not Connect!
39	**3.3V_GND**			
40	**3.3V_GND**			
41	**3.3V**			
42	**3.3V**			
43	**3.3V**			
44	**3.3V**			
45	**3.3V_GND**			
46	**3.3V_GND**			
47	**N.C.**			No Connect
48	**N.C.**			
49	**GND**			
50	***(RX_MCLKn)***	O	CML	For optical waveform testing. Not for normal use.
51	***(RX_MCLKp)***	O	CML	For optical waveform testing. Not for normal use.
52	**GND**			
53	**GND**			

71	**GND**			
72	**RX3p**	O	CML	Output Data
73	**RX3n**	O	CML	Inverted Output Data
74	**GND**			
75	**N.C.**			
76	**N.C.**			
77	**GND**			
78	**(REFCLKp)**			
79	**(REFCLKn)**			

Block diagram



Package outline

Regulatory Compliance

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883E Method 3015.7	high speed signal pins shall withstand 500V electrostatic discharge based on Human Body Model per JEDEC JESD22-A114-B the other pins with exception of the high speed signal pins shall withstand 2kV electrostatic discharge based on Human Body Model per JEDEC JESD22-A114-B

Immunity	IEC61000-4-3 Class 2	Compliant with any electo-magnetic regulations
Safety	FDA CDRH 21-CFR 1040 Class 1	
	UL	
	TUV-GS	
	CE	

Ordering Information

Part No	Specifications				Application Code
	Pack	Data rate	Tx	Pout	