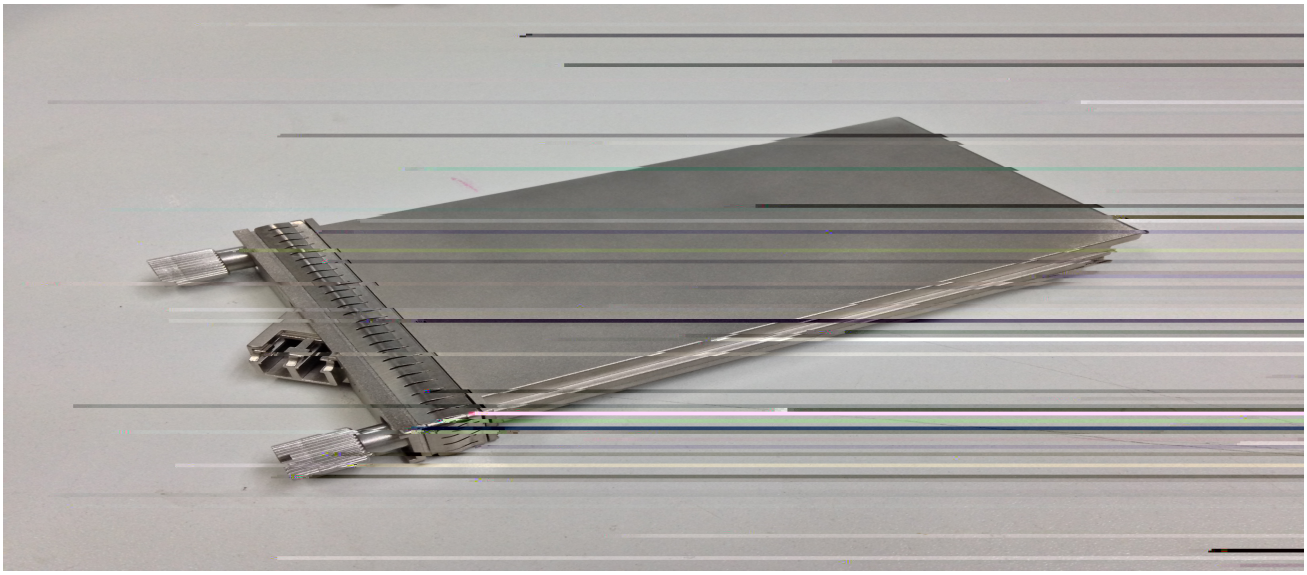

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Pack	Data rate	Tx	Pout	Rx

Resistance					
Differential Signal Input Resistance		Ω	80		120
3.3V LVCMOS Electrical Characteristics					
Input High Voltage	3.3VIH	V	2.0	-	Vcc+0.3
Input Low Voltage	3.3VIL	V	-0.3	-	0.8
Input Leakage Current	3.3IIN	uA	-10	-	+10
Output High Voltage (I_{OH}=100uA)	3.3VOH	V	Vcc-0.2	-	-
Output Low Voltage (I_{OL}=100uA)	3.3VOL	V			0.2
Minimum Pulse Width of Control Pin Signal	t_CNTL	us	100		
1.2V LVCMOS Electrical Characteristics					
Input High Voltage	1.2VIH	V	0.84		1.5
Input Low Voltage	1.2VIL	V	-0.3		0.36
Input Leakage Current	1.2IIN	uA	-100		+100
Output High Voltage	1.2VOH	V	1.0		1.5
Output Low Voltage	1.2VOL	V	-0.3		0.2
Output High Current	1.2IOH	mA			-4
Output Low Current	1.2IOL	mA	+4		
Input Capacitance	Ci	pF			10
Optical transmitter Characteristics					
Signaling Rate for Each Lane （100GbE）					

Lane					
Difference in Receive Power between Any Two Lanes		dBm	-	4.5	
Receiver Sensitivity in OMA for Each Lane(100GbE)	SOMA	dBm		-21.4	8
Receiver Sensitivity in OMA for Each Lane(OTU4)				-23.2	9
Stressed Receiver Sensitivity in OMA for Each Lane(100GbE)		dBm		-17.9	10&11
Los Assert		dBm	-30		
Los De-assert		dBm		-20.9	
Los Hysteresis		dBm	0.5		

The supply current includes CFP module's supply current and test board working current.

Average launch power ,each lane(min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance

Transmitter reflectance is defined looking into the transmitter

The receiver shall be able to tolerate , without damage, continuous exposure to an optical input signal having this average power level

The average receive power , each lane (max) for 100GBASE-ER4 is larger than the 100BASE-ER4 transmitter value to allow compatibility with 100BASE-LR4 units at short distances

Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance

Receiver sensitivity (OMA), each lane (max) is informative

Measured with PRBS 2^{31}-1 for BER=10^{-5}. The BER for the OTU4 application is required to be met only after FEC has been applied.

Measured with conformance test signal at TP3 for BER=10^{-12}

conditions of stressed receiver sensitivity test: vertical eye closure penalty for each lane is 1.8dB;stressed eye J2 jitter for each lane is 0.3UI; stressed eye J9 jitter for each lane is 0.47UI.

The CFP Module support real-time control functions via hardware pins, listed in the following table: Hardware Control Pins

Hardware Control Pins

Pin #	Symbol	Description	I/O	Logic	H	L	Pull-up/down
30	PRG_CNTL1	Programmable Control 1 MSADefault:TRXIC_RSTn , TX&RX ICs reset, "0":reset;"1"	I	3.3V LVCMOS	per CFP MSA Management Interface Specification		Pull-Up Note1
31	PRG_CNTL2	Programmable Control 2 MSADefault :Hardware Interlock LSB	I	3.3V LVCMOS			Pull-Up Note1
32	PRG_CNTL3	Programmable Control 3 MSA Default:Hardware Interlock MSB	I	3.3V LVCMOS			Pull-Up Note1
36	TX_DIS	Transmitter Disable	I	3.3V LVCMOS	Disable	Enable	Pull-Up Note1
37	MOD_LOPWR	Module Low Power Mode	I	3.3V LVCMOS	Low Power	Enable	Pull-Up Note1
39	MOD_RSTn	Module Reset(Invert)	I	3.3V LVCMOS	Enable	Reset	Pull-Down Note2

Pull-Up resistor (4.7KOhm to 10 KOhm) is located within the CFP module

Pull-Down resistor (4.7KOhm to 10 kOhm) is located within the CFP module

The CFP Module supports alarm hardware pins listed in the following table: Hardware Alarm Pins

Hardware Alarm Pins

Pin #	Symbol

Timing Parameters for CFP hardware Signal Pins are listed in the following table.

Timing Parameters for CFP hardware Signal Pins

Parameter	Symbol	Min	Max	Unit	Notes&Conditions
Hardware MOD_LOPWR assert	t_MOD_LOPWR_assert		1	ms	Application Specific May depend on current state Condition when signal is applied .See Vendor Datasheet
Hardware MOD_LOPWR deassert	t_MOD_LOPWR_deassert			ms	Value is dependent upon module start-up time.Please See register"Maximum High-Power-up ime"in "CFP MSA Management Interface Specification"
Receiver Loss of Signal Assert Time	t_loss_assert		100	us	Maximum value designed to support telecom applications
Receiver Loss of Signal De-Assert Time	t_loss_deassert		100	us	Maximum value designed to support telecom applications
Global Alarm Assert Delay Time	GLB_ALRMn_assert		150	ms	This is a logical "OR" of Associated MDIO alarm& status registers.Please see MDIO document for further details
Global Alarm De-assert Delay Time	GLB_ALRMn_deassert		150	ms	This is a logical "OR" of Associated MDIO alarm& status registers.Please see MDIO document for further details
Management Interface Clock Period	t_prd	250		ns	MDC is 4MHz rate
Host MDIO t_setup	t_setup	10		ns	
Host MDIO t_hold	t_hold	10		ns	
CFP MDIO t_delay	t_delay	0	175	ns	
Initialization time from Reset	t_initialize		2.5	s	
Transmitter Disabled(TX_DIS_asserted)	t_deassert		100	us	Application Specific

Transmitter Enabled(TX_DIS_asserted)	t_assert		10	ms	Value is dependent upon module start-up time.Please See register “Maximum TX-Turn-on Time” in “CFP MSA Management Interface Specification”

Reference Clock Characteristics

		Min	Typ	Max	Unit	Notes
Impedance	Zd	80	100	120		

8000	807F	RO	128	8	CFP NVR 1.Basic ID register
8080	80FF	RO	128	8	CFP NVR 2.Extended ID register
8100	817F	RO	128	8	CFP NVR 3. Network lane specific registers
8180	81FF	RO	128	8	CFP NVR 4
8200	83FF	RO	4x128	N/A	MSA Reserved
8400	847F	RO	128	8	Vendor NVR 1. Vendor data registers
8480	84FF	RO	128	8	Vendor NVR 2. Vendor data registers
8500	87FF	RO	6x128	N/A	Reserved by CFP MSA
8800	887F	R/W	128	8	User NVR 1. User data registers
8880	88FF	R/W	128	8	User NVR 2. User data registers
8900	8EFF	RO	12x128	N/A	Reserved by CFP MSA
8F00	8FFF	N/A	2x128	N/A	Reserved for User private use
9000	9FFF	RO	4096	N/A	Reserved for vendor private use
A000	A07F	R/W	128	16	CFP Module VR1. CFP Module level control and DDM registers

8010	1	RO	7~0	Transmitter Spectral Characteristics1		
8011	1	RO	7~0	Transmitter Spectral Characteristics2		
8012	2	RO	7~0	Minimum Wavelength per Active Fiber		
8014	2	RO	7~0	Maximum Wavelength per Active Fibe		
8016	2	RO	7~0	Maximum per Lane Optical Width		
8018	1	RO	7~0	Device Technology1		
8019	1	RO	7~0	Device Technology2		
801A	1	RO	7~0	Signal Code		
801B	1	RO	7~0	Maximum Total Optical Output Power per Connector		
801C	1	RO	7~0	Maximum Optical Input Power per Network Lane		
801D	1	RO	7~0	Maximum Power Consumption		
801E	1	RO	7~0	Maximum Power Consumption in Low Power Mode		
801F	1	RO	7~0	Maximum Operating Case Temp Range		
8020	1	RO	7~0	Minimum Operating Case Temp Range		
8021	16	RO	7~0	Vendor Name		
8031	3	RO	7~0	Vendor OUI		
8034	16	RO	7~0	Vendor Part Number		
8044	16	RO	7~0	Vendor Serial Number		
8054	8	RO	7~0	Data Code		
805C	2	RO	7~0	Lot Code		
805E	10	RO	7~0	CLEI Code		
8068	1	RO	7~0	CFP MSA hardware Specification Revision Number		
8069	1	RO	7~0			

Hex Addr	Size	Access Type	Bit	Register Name	Content (HEX)	LSB Unit
Base ID Information						
8080	2	RO	7~0	Transceiver Temp High Alarm Threshold		
8082	2	RO	7~0	Transceiver Temp High Warning Threshold		
8084	2	RO	7~0	Transceiver Temp Low Warning Threshold		
8086	2	RO	7~0	Transceiver Temp Low Alarm Threshold		
8088	2	RO	7~0	VCC High Alarm Threshold		
808A	2	RO	7~0	VCC High Warning Threshold		
808C	2	RO	7~0	VCC Low Warning Threshold		
808E	2	RO	7~0	VCC Low Alarm Threshold		
8090	2	RO	7~0	[redacted]		
8092	2	RO	7~0	SOA Bias Current High Warning Threshold		
8094	2	RO	7~0	SOA Bias Current Low Warning Threshold		
8096	2	RO	7~0	SOA Bias Current Low Alarm Threshold		
8098	2					

				Threshold		
80C0	2	RO	7~0	Receive Optical Power High Alarm Threshold		
80C2	2	RO	7~0	Receive Optical Power High Warning Threshold		
80C4	2	RO	7~0	Receive Optical Power Low Warning Threshold		
80C6	2	RO	7~0	Receive Optical Power Low Alarm Threshold		
80C8	55	RO	7~0	Reserved		
80FF	1	RO	7~0	CFP NVR 2 Checksum		

Hex Addr	Size	Access Type	Bit	Register Name	Content (HEX)	LSB Unit
Base ID Information						
8100	32	RO	7~0	Rx Sensitivity Spec for network lanes 0~15		
8120	32	RO	7~0	Tx Power Spec for network lanes 0~15		
8140	32	RO	7~0	Measured ER for network lanes 0~15		
8160	32	RO	7~0	Path Penalty for network lanes 0~15		

Hex Addr	Size	Access Type	Bit	Register Name	Content (HEX)	LSB Unit
Base ID Information						
8180	1	RO	7~0	CFP NVR3 Checksum		
8181	127	RO	7~1	Reserved		

Hex Addr	Size	Access Type	Bit	Register Name	Content (HEX)	LSB Unit
Module Command/Setup Registers						
A000	2	RO	15~0	Reserved		
A002	2	RO	15~0	Reserved		
A004	1	RO				
			8~6	Reserved		
			4	Reserved		
			3~2	Command Status		
		RW	15~9	Reserved		
			5	User Restore and Save Command		
			1~0	Extended Commands		
A005	1	RO				
			15~8	Reserved		
		RW	7~0	Function Select Code		
A006	1	RO				
			15~8	Reserved		
		RW	7~0	Function Select Code		
A007	1	RO				
			15~8	Reserved		

		RW	7~0	Function Select Code		
A008	1	RO				
			15~8	Reserved		
		RW	7~0	Alarm Source Code		
A009	1	RO				
			15~8	Reserved		
		RW	7~0	Alarm Source Code		
A00A	1	RO				
			15~8	Reserved		
		RW	7~0	Alarm Source Code		
A00B	1	RO		Module Bi-/Uni-Directional Operating Mode Select		
			15~3	Reserved		
		RW	2~0	Module Bi/uni-Direction Mode Select		
A00C	4	RO		Reserved		
Module Control Registers						
A010	1					
		RW/SC/LH	15	Soft Module Reset		
		RW	14	Soft Module Low Power		
		RW	13	Soft TX Disable		
		RW	12	Soft PRG_CNTL3 Control		
		RW	11	Soft PRG_CNTL2 Control		
		RW	10	Soft PRG_CNTL1 Control		
		RW	9	Soft GLB_ALRM Test		
		RO	8~6	Reserved		
		RO	5	TX_DIS Pin State		
		RO	4			

		RW	7~5	RX MCLK Control		
		RW	4	RX FIFO Reset		
		RW	3~1	RX Rate Select		
		RW	0	RX		

			98	Module Fault Summary		

			5	Lane 5 Fault and Status Summary		
			4	Lane 4 Fault and Status Summary		
			3	Lane 3 Fault and Status Summary		
			2	Lane 2 Fault and Status Summary		
			1	Lane 1 Fault and Status Summary		
			0	Lane 0 Fault and Status Summary		
A01B	1	RO				
			15	Lane 15 Fault and Status Summary		
			14	Lane 14 Fault and Status Summary		
			13	Lane 13 Fault and Status Summary		
			12	Lane 12 Fault and Status Summary		
			11	Lane 11 Fault and Status Summary		
			10	Lane 10 Fault and Status Summary		
			9	Lane 9 Fault and Status Summary		
			8	Lane 8 Fault and Status Summary		
			7	Lane 7 Fault and Status Summary		
			6	Lane 6 Fault and Status Summary		
			5	Lane 5 Fault and Status Summary		
			4	Lane 4 Fault and Status Summary		
			3	Lane 3 Fault and Status Summary		
			2	Lane 2 Fault and Status Summary		
			1	Lane 1 Fault and Status Summary		
			0	Lane 0 Fault and Status Summary		
A01C	1	RO		Reserved		
Module FAWS Registers						
A01D	1	RO				
			15	Reserved		
			14	Reserved		
			13	HW_Interlock		
			12~11	Reserved		
			10	Loss of REFCLK Input		
			9	TX_JITTER_PLL_LOL		
			8	TX_CMU_LOL		
			7	TX_LOSF		
			6	TX_HOST_LOL		
			5	RX_LOS		
			4	RX_NETWORK_LOL		
			3	Out of Alignment		

			2	Reserved		
			1	HIPWR_ON		
			0	Reserved		
A01E	1	RO				
			15	Reserved		
			14~7	Reserved		
			6	PLD or Flash Initialization Fault		
			5	Power Supply Fault		
			4~2	Reserved		
			1	CFP Checksum Fault		
			0	Reserved		
A01F	1	RO				
			15~12	Reserved		
			11	Mod Temp High Alarm		
			10	Mod Temp High Warning		
			9	Mod Temp Low Warning		
			8	Mod Temp Low Alarm		
			7	Mod Vcc High Alarm		
			6	Mod Vcc High Warning		
			5	Mod Vcc Low Warning		
			4	Mod Vcc Low Alarm		
			3	Mod SOA Bias High Alarm		
			2	Mod SOA Bias High Warning		
			1	Mod SOA Bias Low Warning		
			0	Mod SOA Bias Low Alarm		
A020	1	RO				
			15~8	Reserved		
			7	Mod Aux 1 High Alarm		
			6	Mod Aux 1 High Warning		
			5	Mod Aux 1 Low Warning		
			4	Mod Aux 1 Low Alarm		
			3	Mod Aux 2 High Alarm		
			2	Mod Aux 2 High Warning		
			1	Mod Aux 2 Low Warning		
			0	Mod Aux 2 Low Alarm		
A021	1	RO		Reserved		
A022	1					
		RO	15~9	Reserved		
		RO/LH/COR	8	High-Power-down State Latch		
		RO/LH/COR	7	TX-Turn-off State Latch		
		RO/LH/COR	6	Fault State Latch		
		RO/LH/COR	5			

		RO/LH/COR	6	TX_HOST_LOL Latch		
		RO/LH/COR	5	RX_LOS Latch		
		RO/LH/COR	4	RX_NETWORK_LOL Latch		
		RO/LH/COR	3	Out of Alignment Latch		
		RO	2~0	Reserved		
A024	1					
		RO	15~7	Reserved		
		RO/LH/COR	6	PLD or Flash Initialization Fault Latch		
		RO/LH/COR	5	Power Supply Fault Latch		
		RO	4~2	Reserved		
		RO/LH/COR	1	CFP Checksum Fault Latch		
		RO	0	Reserved		
A025	1					
		RO	15~12	Reserved		
		RO/LH/COR	11	Mod Temp High Alarm Latch		
		RO/LH/COR	10	Mod Temp High Warning Latch		
		RO/LH/COR	9	Mod Temp Low Warning Latch		
		RO/LH/COR	8	Mod Temp Low Alarm Latch		
		RO/LH/COR	7	Mod Vcc High Alarm Latch		
		RO/LH/COR	6	Mod Vcc High Warning Latch		
		RO/LH/COR	5	Mod Vcc Low Warning Latch		
		RO/LH/COR	4	Mod Vcc Low Alarm Latch		
		RO/LH/COR	3	Mod SOA Bias High Alarm Latch		
		RO/LH/COR	2	Mod SOA Bias High Warning Latch		
		RO/LH/COR	1	Mod SOA Bias Low Warning Latch		
		RO/LH/COR	0	Mod SOA Bias Low Alarm Latch		
A026	1					
		RO	15~8	Reserved		
		RO/LH/COR	7	Mod Aux 1 High Alarm Latch		
		RO/LH/COR	6	Mod Aux 1 High Warning Latch		
		RO/LH/COR	5	Mod Aux 1 Low Warning Latch		
		RO/LH/COR	4	Mod Aux 1 Low Alarm Latch		
		RO/LH/COR	3	Mod Aux 2 High Alarm Latch		
		RO/LH/COR	2	Mod Aux 2 High Warning Latch		
		RO/LH/COR	1	Mod Aux 2 Low Warning Latch		
		RO/LH/COR	0	Mod Aux 2 Low Alarm Latch		
A027	1	RO		Reserved		
A028	1					
		RO	15~9	Reserved		
		RW	8	High-Power-down State Enable		
		RW	7	TX-Turn-off State Enable		
		RW	6	Fault State Enable		
		RW	5	Ready State Enable		
		RW	4	TX-Turn-on State Enable		
		RW	3	TX-Off State Enable		
		RW	2	High-Power-up State Enable		
		RW	1	Low-Power State Enable		

		RO	0	Initialize State Enable		
A029	1					
		RW	15	GLB_ALRM Master Enable		
		RO	14	Reserved		
		RW	13	HW Interlock		
		RO	12~11	Reserved		
		RW	10	Loss of REFCLK Input Enable		
		RW	9	TX_JITTER_PLL_LOL Enable		
		RW	8	TX_CMU_LOL Enable		
		RW	7	TX_LOSF Enable		
		RW	6	TX_HOST_LOL Enable		
		RW	5	RX_LOS Enable		
		RW	4	RX_NETWORK_LOL Enable		
		RW	3	Out of Alignment Enable		
		RO	2~0	Reserved		
A02A	1					
		RO	15~7	Reserved		
		RW	6	PLD or Flash Initialization Fault Enable		
		RW	5	Power Supply Fault Enable		
		RO	4~2	Reserved		
		RW	1	CFP Checksum Fault Enable		
		RO	0	Reserved		
A02B	1	RO		Module Alarm and Warnings 1 Enable		
			15~12	Reserved		
			11	Mod Temp Hi Alarm Enable		
			10	Mod Temp Hi Warn Enable		
			9	Mod Temp Low Warning Enable		
			8	Mod Temp Low Alarm Enable		
			7	Mod Vcc High Alarm Enable		
			6	Mod Vcc High Warning Enable		
			5	Mod Vcc Low Warning Enable		
			4	Mod Vcc Low Alarm Enable		
			3	Mod SOA Bias High Alarm Enable		
			2	Mod SOA Bias High Warning Enable		
			1	Mod SOA Bias Low Warning Enable		
			0	Mod SOA Bias Low Alarm Enable		
A02C	1					
		RO	15~8	Reserved		
		RW	7	Mod Aux 1 High Alarm Enable		
			6	Mod Aux 1 High Warning Enable		
			5	Mod Aux 1 Low Warning Enable		
			4	Mod Aux 1 Low Alarm Enable		
			3	Mod Aux 2 High Alarm Enable		
			2	Mod Aux 2 High Warning Enable		

			13	Lane APD Power Supply Fault		
			12~8	Reserved		
			7	Lane TX_LOSF		
			6	Lane TX_LOL		
			5	Reserved		
			4	Lane RX_LOS		
			3	Lane RX_LOL		
			2	Lane RX FIFO error		
			1	Reserved		
			0	Reserved		
A220	16	RO/LH/COR				
			15	Bias High Alarm Latch		
			14	Bias High Warning Latch		
			13	Bias Low Warning Latch		
			12	Bias Low Alarm Latch		
			11	TX Power High Alarm Latch		

			10	TX Power High Warning Enable		
			9	TX Power Low Warning Enable		
			8	TX Power Low Alarm Enable		
			7	Laser Temperature High Alarm Enable		
			6	Laser Temperature High Warning Enable		
			5	Laser Temperature Low Warning Enable		
			4	Laser Temperature Low Alarm Enable		
			3	RX Power High Alarm Enable		
			2	RX Power High Warning Enable		
			1	RX Power Low Warning Enable		
			0	RX Power Low Alarm Enable		
A250	16					
		RW	15	Lane TEC Fault Enable		
		RW	14	Lane Wavelength Unlocked Fault Enable		
		RW	13	Lane APD Power Supply Fault Enable		
		RO	12~8	Reserved		
		RW	7	Lane TX_LOSF Enable		
		RW	6	Lane TX_LOL Enable		
		RO	5	Reserved		
		RW	4	Lane RX_LOS Enable		
		RW	3	Lane RX_LOL Enable		
		RW	2	Lane RX FIFO Status Enable		
		RO	1~0	Reserved		
A260	32	RO		Reserved		

Network Lane VR1						
Hex Addr	Size	Access Type	Bit	Register Name	Content (HEX)	LSB Unit
A280	16					
		RW	15~8	Phase Adjustment		
		RW	7~0	Amplitude Adjustment		
A290	16	RO	15~0	Network Lane n PRBS Rx Error Count		
			15~10	Exponent		
			9~0	Mantissa		
A2A0	16	RO	15~0	Network Lane n Laser Bias Current monitor A/D value		
A2B0	16	RO	15~0	Network Lane n Laser Output Power monitor A/D value		

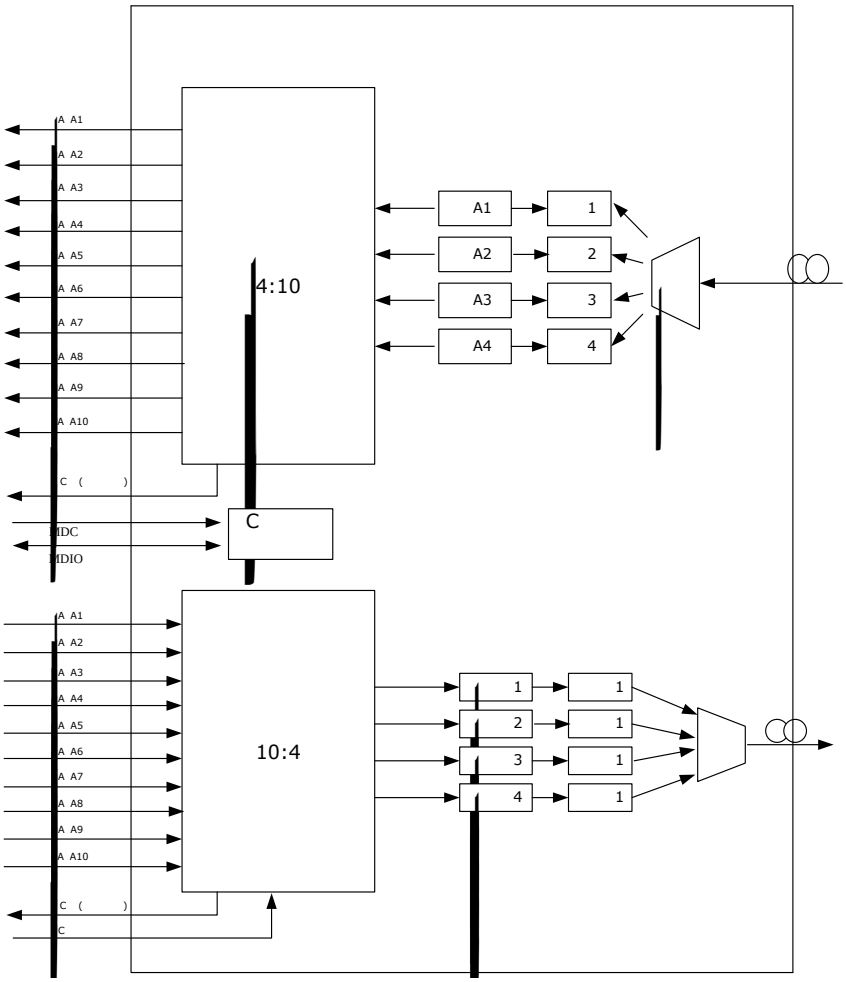
A2C0	16	RO	15~0	Network Lane n Laser Temp Monitor A/D value		
A2D0	16	RO	15~0	Network Lane n Receiver Input Power monitor A/D value		
A2E0	32	RO	15~0	Reserved		

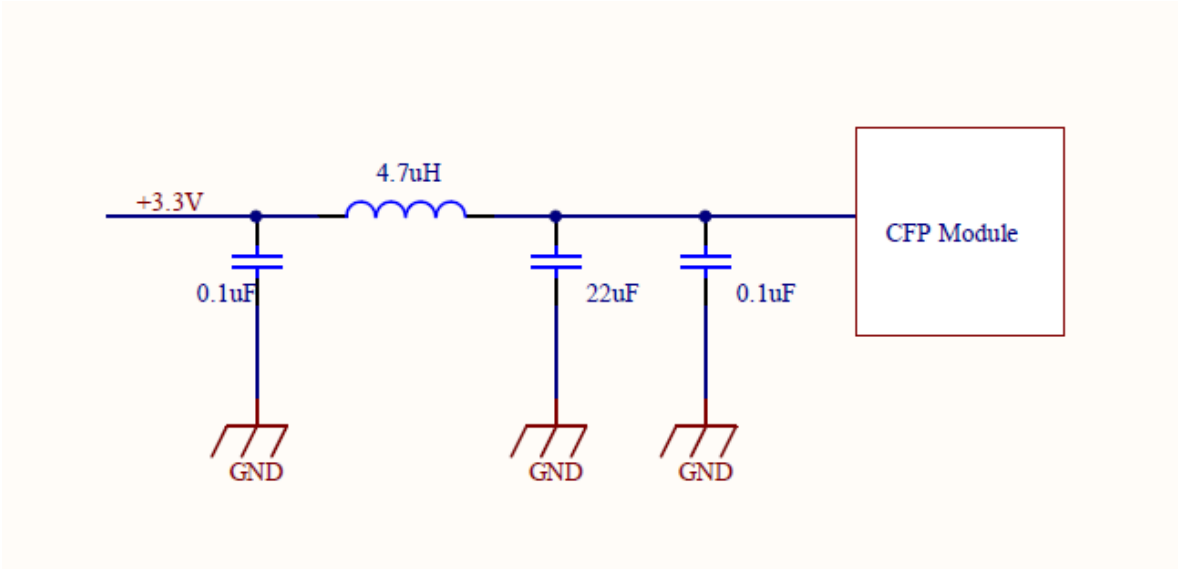
25	TX_MCLKp	O	CML	For optical waveform testing. Not for normal use
26	GND			
27	VND_IO_C	I/O		Module Vendor I/O C. Do Not Connect
28	VND_IO_D	I/O		Module Vendor I/O C. Do Not Connect
29	VND_IO_E	I/O		Module Vendor I/O C. Do Not Connect
30	PRG_CNTL1	I	LVCMOS w/PUR	Programmable Control 1 set over MDIO. MSA Default: TRXIC_RSTn, TX&RX ICs reset,"0" Reset, "1" or NC: enabled=not used
31	PRG_CNTL2	I	LVCMOS w/PUR	Programmable Control 2 set over MDIO. MSA Default: Hardware Interlock LSB, "00"≤8W, "01" ≤16W, "10" ≤24W, "11" or NC≤24W=not used
32	PRG_CNTL3	I	LVCMOS w/PUR	Programmable Control 2 set over MDIO. MSA Default: Hardware Interlock MSB, "00"≤8W, "01" ≤16W, "10" ≤24W, "11" or NC≤24W=not used
33	PRG_ALRM1	O	LVCMOS	Programmable Alarm 1 set over MDIO, MSA Default: HIPWR_ON."1":module power up completed,"0": module not high powered up
34	PRG_ALRM2	O	LVCMOS	Programmable Alarm 2 set over MDIO, MSA Default: MOD_READY, "1": Ready, "0": not Ready
35	PRG_ALRM3	O	LVCMOS	Programmable Alarm 3 set over MDIO, MSA Default: MOD_FAULT, fault detected, "1": Fault, "0": No Fault
36	TX_DIS	I	LVCMOS w/PUR	Transmitter Disable for all lanes, "1" or NC=transmitter disabled,"0"=transmitter enabled
37	MOD_LOPWR	I	LVCMOS w/PUR	Module Low Power Mode."1" or NC: module in low power(safe) mode, "0": power-on enabled
38	MOD_ABS	O	GND	Module Absent "1" or "NC": module absent, "0": module present, Pull Up Resistor in Module
39	MOD_RSTn	I	LVCMOS w/PDR	Module Reset. "0" reset the module, "1" or NC=module enabled, Pull Down Resistor in Module
40	RX_LOS	O	LVCMOS	Receiver Loss of Optical Signal, "1": low optical signal, "0": normal condition

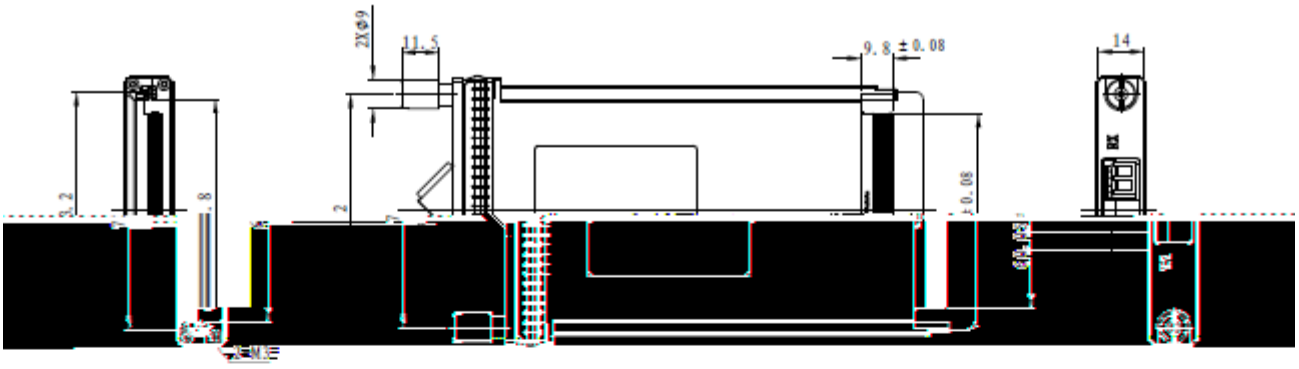
41	GLB_ALRMn	O	LVCMOS	Global Alarm, “0” :alarm condition in any MDIO Alarm register, “1”: no alarm condition, Open Drain, Pull up Resistor on Host
42	PRTADR4	I	1.2V CMOS	MDIO Physical Port address bit4
43	PRTADR3	I	1.2V CMOS	MDIO Physical Port address bit3
44	PRTADR2	I	1.2V CMOS	MDIO Physical Port address bit2
45	PRTADR1	I	1.2V CMOS	MDIO Physical Port address bit1
46	PRTADR0	I	1.2V CMOS	MDIO Physical Port address bit0
47	MDIO	I/O	1.2V CMOS	Management Data I/O bi-directional data (electrical specs as per 802.3ae and ba)
48	MDC	I	1.2V CMOS	Management Data Clock(Electrical specs as per 802.3ae and ba)
49	GND			
50	VND_IO_F	I/O		Module Vendor I/O F. Do Not Connect
51	VND_IO_G	I/O		Module Vendor I/O G. Do Not Connect
52	GND			
53	VND_IO_H	I/O		Module Vendor I/O H. Do Not Connect
54	VND_IO_J	I/O		Module Vendor I/O J. Do Not Connect
55	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal
56	3.3V_GND			
57	3.3V_GND			
58	3.3V_GND			
59	3.3V_GND			
60	3.3V			3.3V Module Supply Votage
61	3.3V			
62	3.3V			
63	3.3V			
64	3.3V			
65	3.3V			
66	3.3V			
67	3.3V			
68	3.3V			
69	3.3V			
70	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal
71	3.3V_GND			
72	3.3V_GND			
73	3.3V_GND			
74	3.3V_GND			
75	GND			

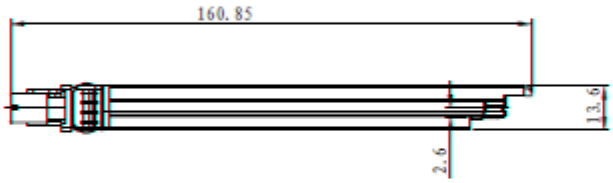
76	RX_MCLKp	O	CML	Receiver Monitor Clock (Optional)
77	RX_MCLKn	O	CML	Receiver Monitor Inverted Clock (Optional)
78	GND			
79	RX0p	O	CML	Output Data
80	RX0n	O	CML	Inverted Output Data
81	GND			
82	RX1p	O	CML	Output Data
83	RX1n	O	CML	Inverted Output Data
84	GND			
85	RX2p	O	CML	Output Data
86	RX2n	O	CML	Inverted Output Data
87	GND			
88	RX3p	O	CML	Output Data
89	RX3n	O	CML	Inverted Output Data
90	GND			

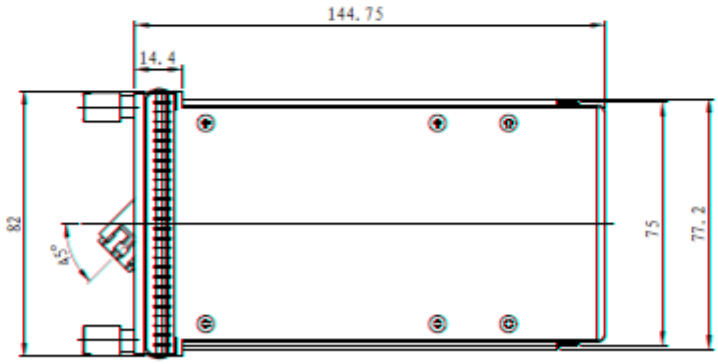
117	TX1n	In	CML	Inverted Input Data
118	GND			
119	TX2p	In	CML	Input Data
120	TX2n	In	CML	Inverted Input Data
121	GND			
122	TX3p	In	CML	Input Data
123	TX3n	In	CML	Inverted Input Data
124	GND			
125	TX4p	In	CML	Input Data
126	TX4n	In	CML	Inverted Input Data
127	GND			
128	TX5p	In	CML	Input Data
129	TX5n	In	CML	Inverted Input Data
130	GND			
131	TX6p	In	CML	Input Data
132	TX6n	In	CML	Inverted Input Data
133	GND			
134	TX7p	In	CML	Input Data
135	TX7n	In	CML	Inverted Input Data
136	GND			
137	TX8p	In	CML	Input Data
138	TX8n	In	CML	Inverted Input Data
139	GND			
140	TX9p	In	CML	Input Data
141	TX9n	In	CML	Inverted Input Data
142	GND			
143	N.C.			
144	N.C.			
145	GND			
146	REFCLKp	In	CML	Reference Input Clock
147	REFCLKn	In	CML	Reference Inverted Input Clock
148	GND			


A A1
A A2
A A3
A A4
A A5
A A6
A A7
A A8
A A9
A A10
C ( )
MDC
MDIO
4:10
C
A1
A2
A3
A4
1
2
3
4
10:4
1
2
3
4
1
1
1
1
C

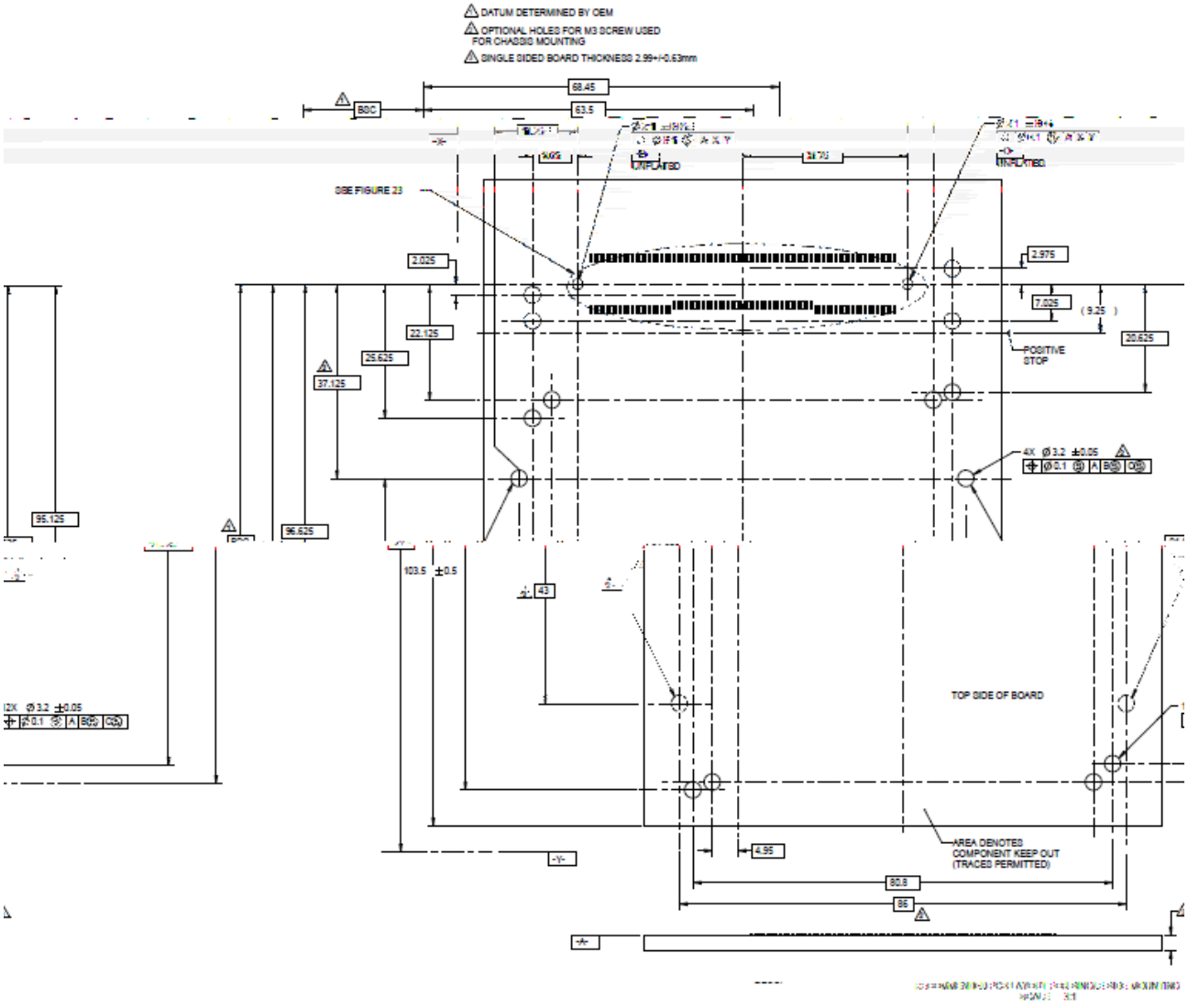

+3.3V
4.7uH
0.1uF
22uF
0.1uF
CFP Module
GND
GND
GND

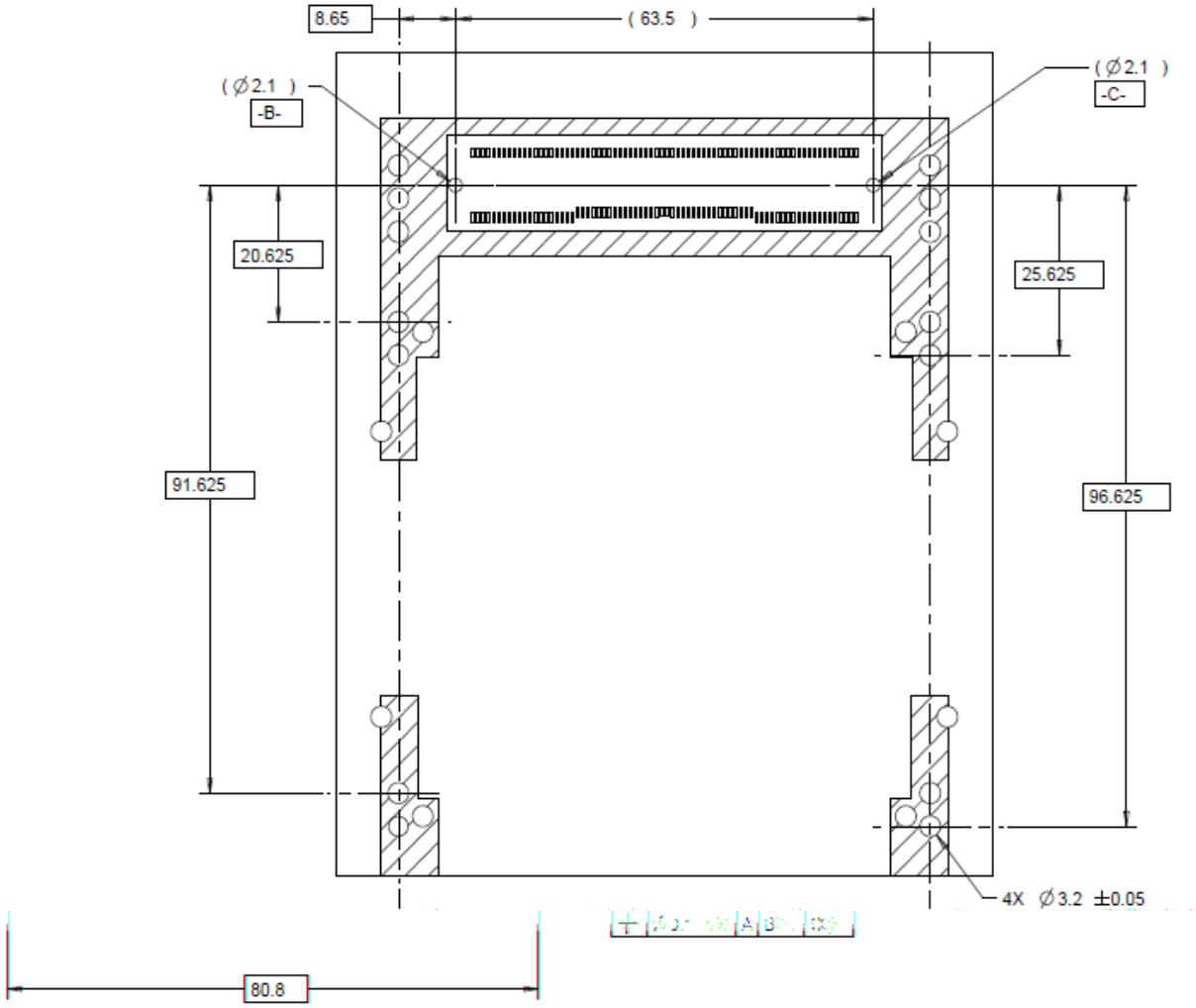






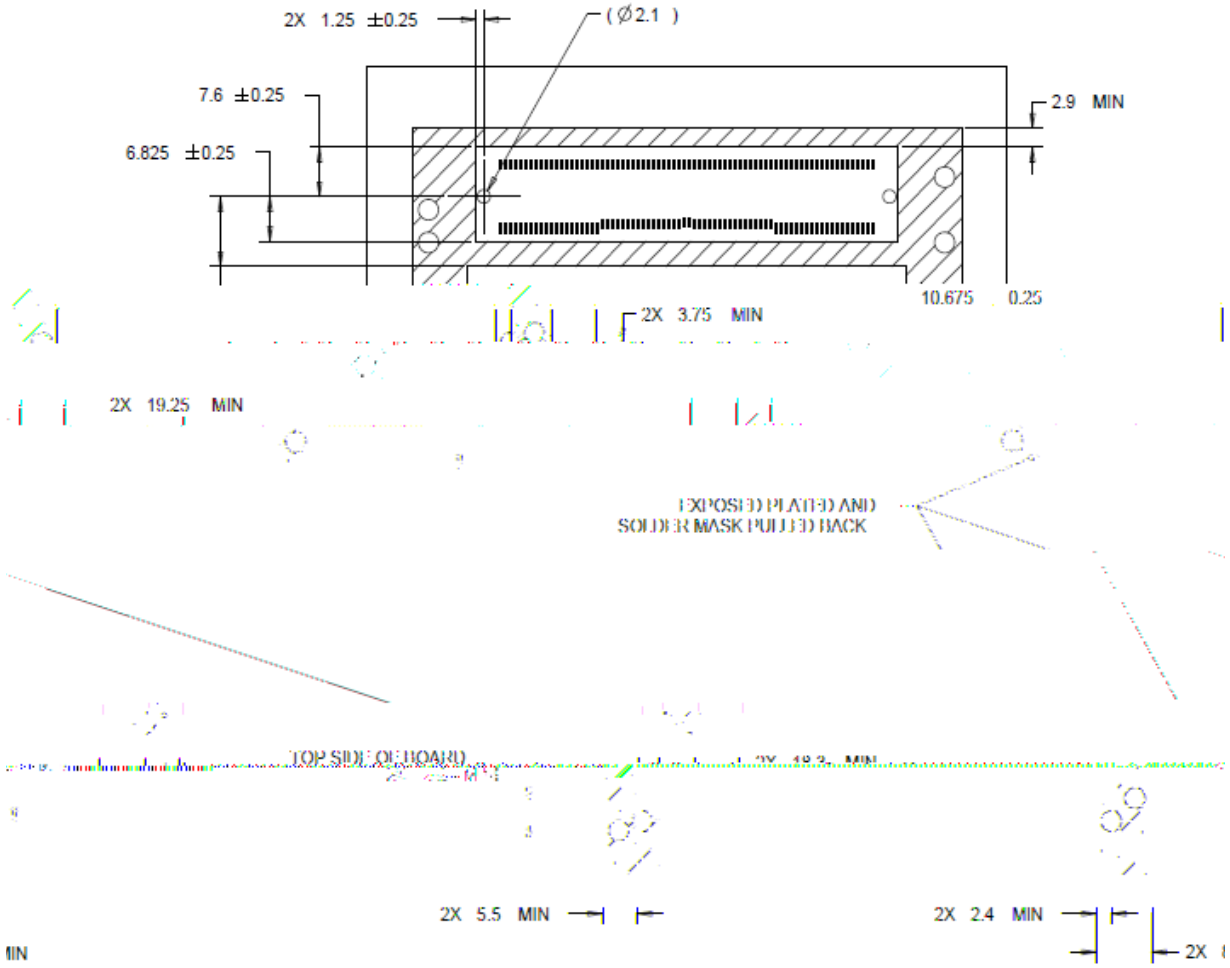
Unit: mm


DATUM DETERMINED BY OEM
OPTIONAL HOLES FOR M3 SCREW USED FOR CHASSIS MOUNTING
SINGLE SIDED BOARD THICKNESS 2.99+/-0.63mm
68.45
63.5
B0C
SEE FIGURE 23
3.025
2.975
7.025
(9.25)
20.625
22.125
25.625
37.125
POSITIVE STOP
95.125
96.625
103.5 ±0.5
43
TOP SIDE OF BOARD
4.95
AREA DENOTED COMPONENT KEEP OUT (TRACES PERMITTED)
80.8
86



BELLY TO BELLY BOARD THICKNESS 3.40+/-0.40mm

FIGURE 21



Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883E Method 3015.7	high speed signal pins shall withstand 500V electrostatic discharge based on Human Body Model per JEDEC JESD22-A114-B the other pins with exception of the high speed signal pins shall withstand 2kV electrostatic discharge based on Human Body Model per JEDEC JESD22-A114-B
Electrostatic Discharge (ESD) Immunity	IEC61000-4-2 Class B	15kV air discharges during operation and 8kV direct contact discharge
Electromagnetic Interference (EMI)	CISPR22 ITE Class B FCC Class B	Compliant with standard

	CENELEC
	EN55022
	VCCI Class 1